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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,686	11/04/2003	Wolfgang Korber	Q78259	4926

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EXAMINER	
WONG, XAVIER S	
ART UNIT	PAPER NUMBER
2609	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/699,686	KORBER ET AL.	
	Examiner	Art Unit	
	Xavier Wong	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4th November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *4th November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4th November 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(A)-(D).

Information Disclosure Statement

The information disclosure statement submitted on *4th November 2003* has been considered by the Examiner and made of record in the application file.

Preliminary Amendment

Acknowledgement is made of applicant's preliminary amendment received on *4th November 2003*.

Drawings

New corrected drawings in compliance with 37 CFR 1.121(D) are required in this application because dark shades in figures *1* through *3* made drawings and its details illegible. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims **11** and **16** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The *burst buffers* in claim **11** are not clearly explained in the specifications or in the claim. Appropriate corrections are required.

The *interactive cascaded* multi-channel network nodes in claim **16** are not clearly explained in the specifications or in the claim. Appropriate corrections are required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (B) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims **1**, **2**, **4 – 8** and **13 – 16** are rejected under 35 U.S.C. 102(B) as being anticipated by **Moriwaki et al (EP 0,918,419 A2)**.

Consider claim **1**, **Moriwaki et al** clearly show and disclose a multi-channel network node (the entire ATM switch system) comprising an ATM switch unit that performs cell distribution and assembling by taking cell data from a plurality of input highways and

pushing the cells through to a plurality of output highways based on destination information in the headers (col. *3* lines *51-58*). The cell distributor routes the cells read into a queue in a buffer memory and cells having the same destination are assigned by an assembler and finally, routed to the same output line of the switch by a demultiplexer (col. *4* lines *1-40*).

Consider claim **2**, and as applied to claim **1** above, **Moriwaki et al** clearly show and disclose when the number of output cells for a same designated switch in parallel is less than the number of switch units, a dummy cell generator will generate *dummy cells* each with the same destination information as the cells and sends the *dummy cells* to the switches for achieving a same/coherent number of cells in each queue to each switch in order to allow the switches to perform same exchange operation independently (col. *4* lines *47-58* & col. *5* lines *1-11*; fig. *1*).

Consider claim **4**, and as applied to claim **1** above, **Moriwaki et al** clearly show and disclose the input of a cell assembly unit is connected to the output of an ATM switch (col. *7* lines *7-30*; fig. *1*). The dummy cell generator, which works as a segmentation unit to distribute the same number of cells in each switch, and the ATM switch unit are coupled to the cell assemblers that comprise the memory buffers (col. *4* lines *42-46* & col. *5* lines *8-10*; *abstract*; fig. *1*).

Consider claim **5**, and as applied to claim **1** above, **Moriwaki et al** clearly show and disclose a cell distributor and a cell assembler comprising a controller unit *34* that controls the cell/memory buffer's queue operations through write address generators (WA) and read address generators (RA) (col. *7* lines *32-50*, col. *11* lines *41-58* & col. *12* lines *1-22*; figs. *4-5* & *9-10*).

Consider claim **6**, and as applied to claim **5** above, **Moriwaki et al** clearly show and disclose the ATM switch system comprising the cell distributor and the cell assembler that handle cells of ATM switches and place them into according memory queues (col. *3* lines *51-58* & col. *4* lines *1-40*; figs. *1*, *4-5* & *9-10*).

Consider claim **7**, and as applied to claim **5** above, **Moriwaki et al** clearly show and disclose each cell distributor and each cell assembler, which both comprise the memory queues, perform exchange operations independently (asynchronously) with the ATM switches (col. *4* lines *15-40*; *abstract*).

Consider claim **8**, and as applied to claim **1** above, **Moriwaki et al** clearly show and disclose the ATM switching unit's capacity can be freely expanded from N x N into a KN x KN (K is a positive integer) by a matrix connection method (col. *6* lines *6-46* & col. *13* lines *40-57*; figs. *1*, *2* & *12*).

Consider claim **9**, and as applied to claim **1** above, **Moriwaki et al** clearly show and disclose a control unit outputs write address, stores cell in buffer, outputs read address to assist transfer of cells from input highways to output highways. Therefore, a software is inherently embedded inside the control unit/processor (col. *11* lines *41-52* & col. *12* lines *7-18*; claim *2*). Therefore, software – coded instructions (programs) that make a system work – is inherently in the control/processor unit in order for the store, read and write instructions to happen.

Consider claim **10**, and as applied to claim **1** above, **Moriwaki et al** clearly show and disclose cells received from an input highway by a cell distributor are distributed from the buffer memory to an input line of an ATM switch unit (col. *4* lines *15-19*; figs. *4-5*). The demultiplexer in the cell assembler takes output queues from the buffer and directs the cells to their specified output highways 50-n (col. *11* lines *52-58* & col. *12* lines *1-22*; figs. *9-10*).

Consider claim **11**, and as applied to claim **1** above, **Moriwaki et al** clearly show and disclose the cell distributor comprises of a structure called queue selector to prevent traffic delays by selecting queue buffers 23-1 through 23-N (col. *13* lines *9-39*); therefore, achieving continuous transfer of data among inputs and outputs with little or no interruption as a operating as a burst buffer (in burst mode).

Consider claim **12**, and as applied to claim **11** above, **Moriwaki et al** clearly show and disclose the outputs of the cell distributor, which embodies memory buffer queues, are coupled to the ATM switching units (col. *4* lines *15-19*; figs. *1* & *4-5*).

Consider claim **13**, and as applied to claim **1** above, **Moriwaki et al** clearly show and disclose the outputs of the cell assembler, which embodies memory buffers, links to the output highways of the ATM switch system (col. *11* lines *52-58* & col. *12* lines *1-22*; figs. *9-10*), which is the network node.

Consider claim **14**, **Moriwaki et al** clearly show and disclose a method for routing/switching data from any input ports to any of a number of output ports of a network node (the entire ATM switch system) (col. *4* lines *15-40*, col. *11* lines *52-58* & col. *12* lines *1-22*; *abstract*) comprising an ATM switch unit that performs cell distribution and assembling by inputting cell data from a plurality of input highways and routing the cells through to a plurality of output highways based on destination information in the headers (col. *3* lines *51-58*; fig. *1*). The cell distributor routes the cells read into queues in memory buffers (cell buffer units) and cells having the same destination are assigned by an assembler and finally, routed to the same output line of the switch by a demultiplexer to the output highways (col. *4* lines *1-40*; figs. *4-5* & *9-10*).

Consider claim **15**, and as applied to claim **14** above, **Moriwaki et al** clearly show and disclose when the number of output cells for a same designated switch in

parallel is less than the number of switch units, a dummy cell generator will generate *dummy cells* each with the same destination information as the cells and sends the *dummy cells* to the switches for achieving a same/coherent number of cells in each queue to each switch in order to allow the switches to perform same exchange operation independently (col. *4* lines *47-58* & col. *5* lines *1-11*; fig. *1*).

Consider claim **16**, and as applied to claim **1** above, **Moriwaki et al** clearly show and disclose the different levels of inputs and outputs in the ATM switch system from the input highways of the cell distributors to the ATM switches to the output highways of the cell assemblers; therefore, creating a cascade of devices operating in a succession of stages (col. *3* lines *52-58* & col. *4* lines *1-46*; fig. *1*). The ATM switch units exchange (interaction) cells with other ATM switch units in an N x N switch matrix (col. *6* lines *6-39*; *abstract*; fig. *1*).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim **3** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Moriwaki et al** (**EP 0,918,419 A2**) in view of **Li et al** (**U.S Patent 5,757,771**).

Consider claim **3**, and as applied to claim **1** above, **Moriwaki et al** clearly show and disclose the claimed invention except the number of memory cells is resizable in order to redistribute buffer capacity of the memory queues.

In a related field of endeavor, **Li et al** disclose a buffer management method for an ATM switch to dynamically set queue lengths of different input data (col. *4* lines *7-11*). The memory buffer is divided into sub-queues distinguished by certain priority/class

levels of the cells and dynamically apportioned to be equal length necessary to hold data of a particular type at all times (col. 4 lines 16-24).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to incorporate the teachings of having the number of memory cells is resizable in order to redistribute buffer capacity of the memory queues as taught by **Li et al**, in the network node of **Moriwaki et al**, in order to maximize buffer memory usage.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

A.) **Folkert de Vries** (**U.S Patent 5,381,409**) mention a switching system in which buffers reside at the output end of every switch matrix row as a result of speeding up register throughput.

Any response to this Office Action should be **faxed to** (571) 273-8300 **or mailed to**:

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P.O. Box 1450
Alexandria, VA 22313-1450

Hand-delivered responses should be **brought to**:

Customer Service Window
Randolph Building
401 Dulany Street

Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Xavier Wong whose telephone number is (571) 270-1780. The examiner can normally be reached on Monday through Friday 8 am - 5 pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rafael Perez-Gutierrez can be reached on (571) 272-7915. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call (800) 786-9199 (IN USA OR CANADA) or (571) 272-1000.

Xavier S. Wong
X.S.W/xsw
23rd March 2007